TYPES 2N3903, 2N3904, A5T3903, A5T3904
N-P-N SILICON TRANSISTORS

*switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS†			2N3903 A5T3903 MAX	2N3904 A5T3904 MAX	UNIT
t_d	Delay Time	I_C = 10 mA,	$I_{B(1)}$ = 1 mA,	$V_{BE(off)}$ = −0.5 V,	35	35	ns
t_r	Rise Time	R_L = 275 Ω,		See Figure 1	35	35	ns
t_s	Storage Time	I_C = 10 mA,	$I_{B(1)}$ = 1 mA,	$I_{B(2)}$ = −1 mA,	175	200	ns
t_f	Fall Time	R_L = 275 Ω,		See Figure 2	50	50	ns

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters. Nominal base current for delay and rise times is calculated using the minimum value of V_{BE}. Nominal base currents for storage and fall times are calculated using the maximum value of V_{BE}.

*The asterisk identifies JEDEC registered data for the 2N3903 and 2N3904 only.

PARAMETER MEASUREMENT INFORMATION

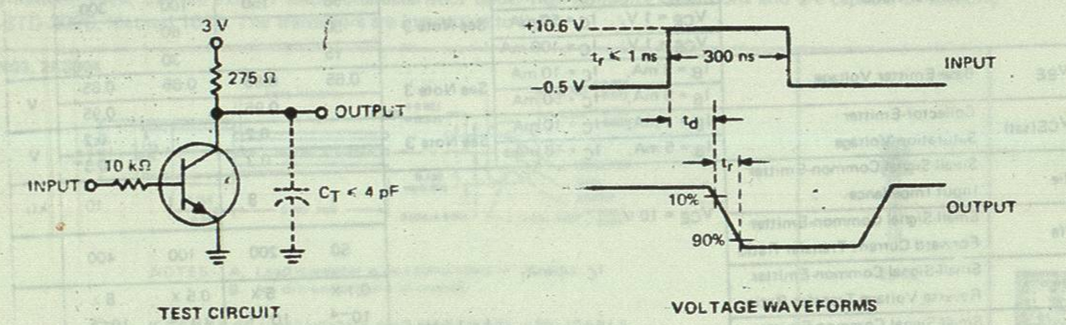

FIGURE 1–DELAY AND RISE TIMES

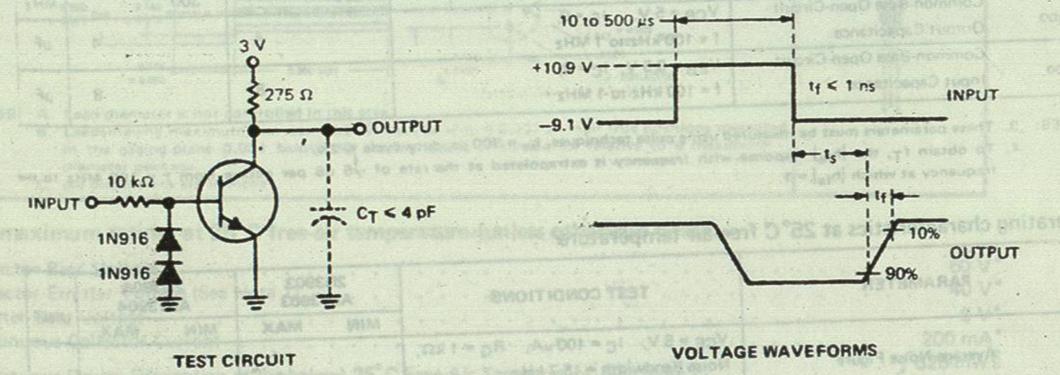

FIGURE 2–STORAGE AND FALL TIMES

NOTES: a. The input waveforms are supplied by a generator with the following characteristics: Z_{out} = 50 Ω, duty cycle ≈ 2%.
b. Waveforms are monitored on an oscilloscope with the following characteristics: t_r ≤ 1 ns, R_{in} ≥ 10 MΩ, C_{in} ≤ 4 pF.

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TYPES 2N3905, 2N3906, A5T3905, A5T3906
P-N-P SILICON TRANSISTORS

BULLETIN NO. DL-S 7311677, NOVEMBER 1971–REVISED MARCH 1973

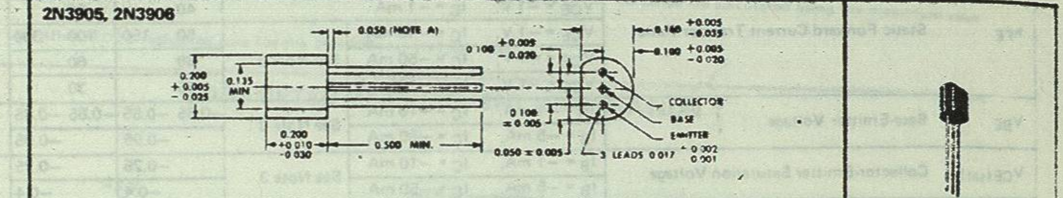
SILECT† TRANSISTORS‡
FOR GENERAL PURPOSE SATURATED-SWITCHING AND AMPLIFIER APPLICATIONS

- For Complementary Use with N-P-N Types 2N3903, 2N3904, A5T3903, and A5T3904
- Rugged One-Piece Construction with In-Line Leads or Standard TO-18 100-mil Pin-Circle Configuration

mechanical data

These transistors are encapsulated in a plastic compound specifically designed for this purpose, using a highly mechanized process developed by Texas Instruments. The case will withstand soldering temperatures without deformation. These devices exhibit stable characteristics under high-humidity conditions and are capable of meeting MIL-STD-202C, Method 106B. The transistors are insensitive to light.

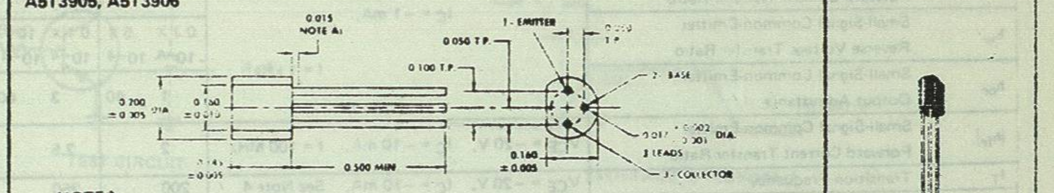
2N3905, 2N3906



NOTES: A. Lead diameter is not controlled in this area.
B. All dimensions are in inches.

*ALL JEDEC TO-92 DIMENSIONS AND NOTES ARE APPLICABLE

A5T3905, A5T3906



NOTES:
A. Lead diameter is not controlled in this area.
B. Leads having maximum diameter (0.019) shall be within 0.007 of their true positions measured in the gaging plane 0.054 below the seating plane of the device relative to a maximum diameter package.
C. All dimensions are in inches.

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absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Collector-Base Voltage	−40 V*
Collector-Emitter Voltage (See Note 1)	−40 V*
Emitter-Base Voltage	−5 V*
Continuous Collector Current	−200 mA*
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 2)	625 mW§ / 310 mW*
Storage Temperature Range	−65°C to 150°C§ / −55°C to 135°C*
Lead Temperature 1/16 Inch from Case for 60 Seconds	260°C§ / 230°C*

NOTES: 1. This value applies between 10 μA and 200 mA collector current when the base-emitter diode is open-circuited.
2. Derate the 625-mW rating linearly to 150°C free-air temperature at the rate of 5 mW/°C. Derate the 310-mW (JEDEC registered) rating linearly to 135°C free-air temperature at the rate of 2.81 mW/°C.

*The asterisk identifies JEDEC registered data for the 2N3905 and 2N3906 only. This data sheet contains all applicable registered data in effect at the time of publication.
†Trademark of Texas Instruments
‡U.S. Patent No. 3,439,238
§Texas Instruments guarantees these values in addition to the JEDEC registered values which are also shown.

USES CHIP P15

TYPES 2N3905, 2N3906, A5T3905, A5T3906 P-N-P SILICON TRANSISTORS

*electrical characteristics at 25°C free-air temperature

	PARAMETER	TEST CONDITIONS			2N3905 A5T3905 MIN	2N3905 A5T3905 MAX	2N3906 A5T3906 MIN	2N3906 A5T3906 MAX	UNIT
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	$I_C = -10\ \mu A$,	$I_E = 0$		−40		−40		V
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	$I_C = -1$ mA,	$I_B = 0$,	See Note 3	−40		−40		V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	$I_E = -10\ \mu A$,	$I_C = 0$		−5		−5		V
I_{CEV}	Collector Cutoff Current	$V_{CE} = -30$ V,	$V_{BE} = 3$ V			−50		−50	nA
I_{BEV}	Base Cutoff Current	$V_{CE} = -30$ V,	$V_{BE} = 3$ V			50		50	nA
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = -1$ V,	$I_C = -100\ \mu A$		30		60		
		$V_{CE} = -1$ V,	$I_C = -1$ mA		40		80		
		$V_{CE} = -1$ V,	$I_C = -10$ mA	See Note 3	50	150	100	300	
		$V_{CE} = -1$ V,	$I_C = -50$ mA		30		60		
		$V_{CE} = -1$ V,	$I_C = -100$ mA		15		30		
V_{BE}	Base-Emitter Voltage	$I_B = -1$ mA,	$I_C = -10$ mA	See Note 3	−0.65	−0.85	−0.65	−0.85	V
		$I_B = -5$ mA,	$I_C = -50$ mA			−0.95		−0.95	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_B = -1$ mA,	$I_C = -10$ mA	See Note 3		−0.25		−0.25	V
		$I_B = -5$ mA,	$I_C = -50$ mA			−0.4		−0.4	
h_{ie}	Small-Signal Common-Emitter Input Impedance	$V_{CE} = -10$ V,	$I_C = -1$ mA,	f = 1 kHz	0.5	8	2	12	kΩ
h_{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio				50	200	100	400	
h_{re}	Small-Signal Common-Emitter Reverse Voltage Transfer Ratio				0.1×10^{-4}	5×10^{-4}	0.1×10^{-4}	10×10^{-4}	
h_{oe}	Small-Signal Common-Emitter Output Admittance				1	40	3	60	μmho
$\|h_{fe}\|$	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -20$ V,	$I_C = -10$ mA,	f = 100 MHz	2		2.5		
f_T	Transition Frequency	$V_{CE} = -20$ V,	$I_C = -10$ mA,	See Note 4	200		250		MHz
C_{obo}	Common-Base Open-Circuit Output Capacitance	$V_{CB} = -5$ V,	$I_E = 0$,	f = 100 kHz to 1 MHz		4.5		4.5	pF
C_{ibo}	Common-Base Open-Circuit Input Capacitance	$V_{EB} = -0.5$ V,	$I_C = 0$,	f = 100 kHz to 1 MHz		10		10	pF

NOTES: 3. These parameters must be measured using pulse techniques. $t_w = 300\ \mu s$, duty cycle ≤ 2%.

4. To obtain f_T, the $|h_{fe}|$ response is extrapolated at the rate of −6 dB per octave from f = 100 MHz to the frequency at which $|h_{fe}| = 1$.

*operating characteristics at 25°C free-air temperature

	PARAMETER	TEST CONDITIONS	2N3905 A5T3905 MIN	2N3905 A5T3905 MAX	2N3906 A5T3906 MIN	2N3906 A5T3906 MAX	UNIT
NF	Average Noise Figure	$V_{CE} = -5$ V, $I_C = -100\ \mu A$, $R_G = 1$ kΩ, Noise Bandwidth = 15.7 kHz, See Note 5		5		4	dB

NOTE 5: Average Noise Figure is measured in an amplifier with response down 3 dB at 10 Hz and 10 kHz and a high-frequency rolloff of 6 dB/octave.

*The asterisk identifies JEDEC registered data for the 2N3905 and 2N3906 only.

TYPES 2N3905, 2N3906, A5T3905, A5T3906 P-N-P SILICON TRANSISTORS

*switching characteristics at 25°C free-air temperature

	PARAMETER	TEST CONDITIONS†	2N3905 A5T3905 MAX	2N3906 A5T3906 MAX	UNIT
t_d	Delay Time	$I_C = -10$ mA, $I_{B(1)} = -1$ mA, $V_{BE(off)} = 0.5$ V, $R_L = 275\ \Omega$, See Figure 1	35	35	ns
t_r	Rise Time		35	35	ns
t_s	Storage Time	$I_C = -10$ mA, $I_{B(1)} = -1$ mA, $I_{B(2)} = 1$ mA, $R_L = 275\ \Omega$, See Figure 2	200	225	ns
t_f	Fall Time		60	75	ns

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters. Nominal base current for delay and rise times is calculated using the minimum value of V_{BE}. Nominal base currents for storage and fall times are calculated using the maximum value of V_{BE}.

*The asterisk identifies JEDEC registered data for the 2N3905 and 2N3906 only.

PARAMETER MEASUREMENT INFORMATION

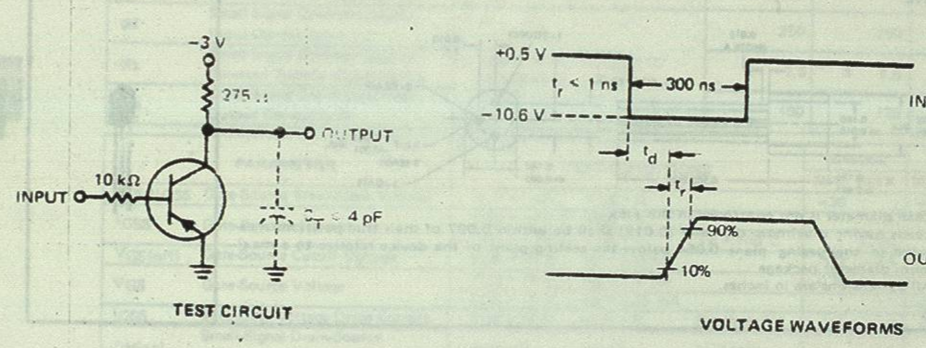


FIGURE 1—DELAY AND RISE TIMES

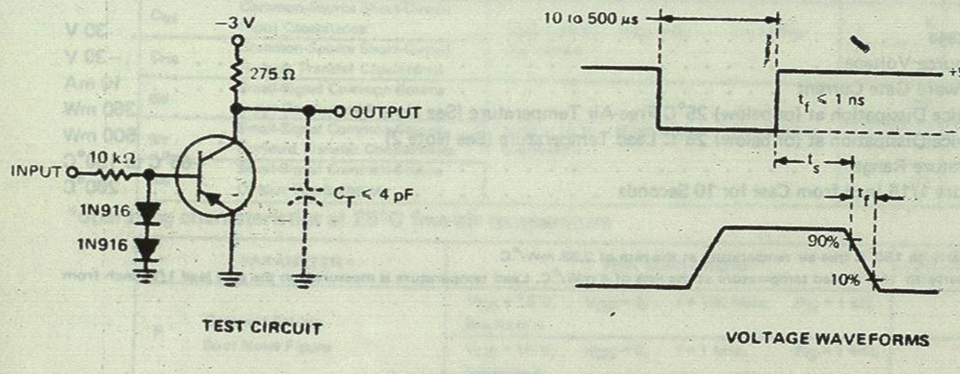


FIGURE 2—STORAGE AND FALL TIMES

NOTES: a. The input waveforms are supplied by a generator with the following characteristics: $Z_{out} = 50\ \Omega$, duty cycle = 2%.

b. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 1$ ns, $R_{in} = 10$ MΩ, $C_{in} \leq 4$ pF.

TYPES 2N5949 THRU 2N5953
N-CHANNEL SILICON JUNCTION FIELD-EFFECT TRANSISTORS

BULLETIN NO. DL-S 7011338, APRIL 1970

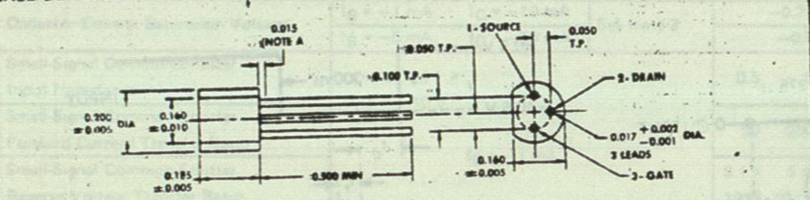
SILECT† FIELD-EFFECT TRANSISTORS‡

- Narrow I_{DSS} and $V_{GS(off)}$ Ranges
- For Low-Noise Audio-Frequency Amplifier Applications
- For RF Amplifier Applications Thru 100 MHz
- Low $r_{ds(on)}$ for Chopper and Switching Applications

mechanical data

These transistors are encapsulated in a plastic compound specifically designed for this purpose, using a highly mechanized process developed by Texas Instruments. The case will withstand soldering temperatures without deformation. These devices exhibit stable characteristics under high-humidity conditions and are capable of meeting MIL-STD-202C Method 106B. The transistors are insensitive to light.

*CASE OUTLINE



NOTES A. Lead diameter is not controlled in this area.
B. Leads having maximum diameter (0.019) shall be within 0.007 of their true positions measured in the gaging plane 0.054 below the seating plane of the device relative to a maximum diameter package.
C. All dimensions are in inches.

*absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Drain-Gate Voltage	30 V
Reverse Gate-Source Voltage	−30 V
Continuous Forward Gate Current	10 mA
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 1)	360 mW
Continuous Device Dissipation at (or below) 25°C Lead Temperature (See Note 2)	500 mW
Storage Temperature Range	−65°C to 150°C
Lead Temperature 1/16 Inch from Case for 10 Seconds	260°C

NOTES: 1. Derate linearly to 150°C free-air temperature at the rate of 2.88 mW/°C.
2. Derate linearly to 150°C lead temperature at the rate of 4 mW/°C. Lead temperature is measured on the gate lead 1/16 inch from the case.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.
†Trademark of Texas Instruments.
‡U.S. Patent No. 3,439,238

USES CHIP JN51

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TYPES 2N5949 THRU 2N5953
N-CHANNEL SILICON JUNCTION FIELD-EFFECT TRANSISTORS

*electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		2N5949 MIN	2N5949 MAX	2N5950 MIN	2N5950 MAX	2N5951 MIN	2N5951 MAX	UNIT
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	$I_G = -1\ \mu A$,	$V_{DS} = 0$	−30		−30		−30		V
I_{GSS}	Gate Reverse Current	$V_{GS} = -15$ V,	$V_{DS} = 0$		−1		−1		−1	nA
		$V_{GS} = -15$ V, $T_A = 100°C$	$V_{DS} = 0$,		−200		−200		−200	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 15$ V,	$I_D = 100$ nA	−3	−7	−2.5	−6	−2	−5	V
V_{GS}	Gate-Source Voltage	$V_{DS} = 15$ V,	$I_D = 1.2$ mA	−2.25	−6					V
		$V_{DS} = 15$ V,	$I_D = 1$ mA			−1.8	−5			
		$V_{DS} = 15$ V,	$I_D = 0.7$ mA					−1.3	−4.5	
I_{DSS}	Zero-Gate-Voltage Drain Current	$V_{DS} = 15$ V, See Note 3	$V_{GS} = 0$,	12	18	10	15	7	13	mA
$r_{ds(on)}$	Small-Signal Drain-Source On-State Resistance	$V_{GS} = 0$, f = 1 kHz	$I_D = 0$,		200		210		250	Ω
$\|y_{fs}\|$	Small-Signal Common-Source Forward Transfer Admittance	$V_{DS} = 15$ V, f = 1 kHz,	$V_{GS} = 0$, See Note 4	3.5	7.5	3.5	7.5	3.5	6.5	mmho
$\|y_{os}\|$	Small-Signal Common-Source Output Admittance				75		75		75	μmho
C_{iss}	Common-Source Short-Circuit Input Capacitance	$V_{DS} = 15$ V, f = 1 MHz,	$V_{GS} = 0$, See Note 4		6		6		6	pF
C_{rss}	Common-Source Short-Circuit Reverse Transfer Capacitance				2		2		2	pF
g_{is}	Small-Signal Common-Source Input Conductance	$V_{DS} = 15$ V, f = 100 MHz,	$V_{GS} = 0$, See Note 4		250		250		250	μmho
g_{fs}	Small-Signal Common-Source Forward Transfer Conductance			3	7.5	3	7.5	3	6.5	mmho
g_{os}	Small-Signal Common-Source Output Conductance				150		125		100	μmho

PARAMETER		TEST CONDITIONS	2N5952 MIN	2N5952 MAX	2N5953 MIN	2N5953 MAX	UNIT
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	$I_G = -1\ \mu A$, $V_{DS} = 0$	−30		−30		V
I_{GSS}	Gate Reverse Current	$V_{GS} = -15$ V, $V_{DS} = 0$		−1		−1	nA
		$V_{GS} = -15$ V, $V_{DS} = 0$, $T_A = 100°C$		−200		−200	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 15$ V, $I_D = 100$ nA	−1.3	−3.5	−0.8	−3	V
V_{GS}	Gate-Source Voltage	$V_{DS} = 15$ V, $I_D = 0.4$ mA	−0.75	−3			V
		$V_{DS} = 15$ V, $I_D = 0.25$ mA			−0.5	−2.5	
I_{DSS}	Zero-Gate-Voltage Drain Current	$V_{DS} = 15$ V, $V_{GS} = 0$, See Note 3	4	8	2.5	5	mA
$r_{ds(on)}$	Small-Signal Drain-Source On-State Resistance	$V_{GS} = 0$, $I_D = 0$, f = 1 kHz		300		375	Ω
$\|y_{fs}\|$	Small-Signal Common-Source Forward Transfer Admittance	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1 kHz, See Note 4	2	6.5	2	6.5	mmho
$\|y_{os}\|$	Small-Signal Common-Source Output Admittance			50		50	μmho
C_{iss}	Common-Source Short-Circuit Input Capacitance	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1 MHz, See Note 4		6		6	pF
C_{rss}	Common-Source Short-Circuit Reverse Transfer Capacitance			2		2	pF
g_{is}	Small-Signal Common-Source Input Conductance	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 100 MHz, See Note 4		250		250	μmho
g_{fs}	Small-Signal Common-Source Forward Transfer Conductance		1	6.5	1	6.5	mmho
g_{os}	Small-Signal Common-Source Output Conductance			75		50	μmho

*operating characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	ALL TYPES MIN	ALL TYPES MAX	UNIT
F	Common-Source Spot Noise Figure	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 100 MHz, $R_G = 1$ kΩ, See Note 4		5	dB
		$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1 kHz, $R_G = 1$ MΩ, See Note 4		2	
V_n	Equivalent Input Noise Voltage	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1 kHz, See Note 4		100	nV/√Hz

NOTES: 3. This parameter must be measured using pulse techniques. $t_w = 300\ \mu s$, duty cycle ≤ 2%.
4. These parameters must be measured with bias conditions applied for less than 5 seconds to avoid overheating.

*JEDEC registered data

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